

FDL'02



FORUM on Specification & Design Languages

Advance Program

September 24-27, 2002



ESIM
Marseille - France

.. Welcome to FDL'02 ..

The Forum on specification & Design Languages (FDL) is the European forum to exchange experiences and learn of new trends in the application of languages and their associated design methods and tools for the design of complex electronic systems. By offering several co-located events, this multi-faceted forum gives an excellent opportunity to gain up-to-date knowledge across a wide field.

FDL'02 is the fifth in a series after Lausanne, Lyon, Tuebingen and ENS Lyon.

This year, the ESIM in Marseille has been chosen to host FDL'02. The venue is located in the north of Marseille and represents an excellent place for such an event.

The forum is organized around four interrelated workshops with tutorials, panels, working sessions, poster sessions, technical presentations and technical discussions within standardization and user group meetings.

The four workshops address key aspects of system-level specification and design:

AMS: Languages for Analog & Mixed-Signal System Design addresses areas like AMS behavioural specification, analog synthesis, mixed-signal simulation, AMS reuse, library development, MEMS, RF, etc. The aim of this workshop is to present new research activities as well as practical experiences, and to exchange ideas in those areas.

CSD: C/C++-Based System Design, presents and discusses C/C++-based design methods and tools around HW/SW co-design, RTOS aspects, simulation, performance evaluation and analysis. Roadmaps for the future development of existing approaches will be presented and discussed.

UML: UML-Based System Specification & Design, presents experiences on UML-based methods for embedded system design, to explore the applicability and required support, and to stimulate the exchange of ideas between communities.

SFP: Specification Formalisms for Proven Design aims at developing an industry-wide consensus on problems met by the designers of electronic systems and systems on chip, namely: system-level specification formalisms, proven verification/refinement, translation of informal specifications to formal ones, task/resource allocation, temporal specifications, architecture languages, proven HW/SW co-design, functional and implementation constraints, design patterns and design flows, EDA tool support, etc.

The program this year fully accomplishes all these goals. I encourage you not to miss this unique opportunity to learn about and contribute to the latest research activities and evolution of system specification languages.



Eugenio Villar
General Chair

..... Programme Sub-Committees

AMS - Languages for Analog & Mixed-Signal System Design

- Peter Schwarz (prog chair)
- Ernst Christen
- Christoph Grimm
- Joachim Haase
- Yannick Hervé
- Tom J. Kazmierski
- H. Alan Mantooth
- Natividad Martinez Madrid
- Guido Schumacher
- Alain Vachoux
- Reimund Wittmann

CSD - C/C++-Based System Design

- Wolfgang Rosenstiel (prog chair)
- Massimo Bombana
- Patrizia Cavallo
- George Economakos
- Norbert Fristacky
- Masahiro Fujita
- Serge Maginot
- Adam Morawiec
- Wolfgang Nebel
- Martin Radetzki
- Franz Rammig
- Jürgen Ruf
- Donatella Sciuto

UML - UML-Based System Specification & Design

- Gjalte de Jong (prog chair)
- Grant Martin
- Jeroen Voeten
- Piet van der Putten
- Bernd Kleinjohann
- Martyn Edwards
- Jean-Louis Sourrouille
- Michael G. Harbour

SFP - Specification Formalisms for Proven Design

- Michael Butler (prog chair)
- Jean Mermet (org chair)
- Perry Alexander
- Peter Ashenden
- Dominique Cansell
- Carlos Delgado Kloos
- Hans Eveking
- Norbert Fristacky
- Kamal Hashmi
- Axel Jantsch
- Klaus Kronlof
- Thierry Lecomte
- Pierre Lescanne
- Wolfgang Mueller
- Roberto Passerone
- Laurence Pierre
- Franz Rammig

... Keynote and tutorial presenters



Christoph Grimm has studied Computer Engineering at the Technical University Darmstadt and the Ecole Centrale de Lyon. He received a Ph. D. for his work on specification and synthesis of mixed-signal systems from the University of Frankfurt in 1999. His research interests include specification and design of mixed-signal systems as well as domain-specific techniques for the acceleration of analog simulations



Karsten Einwich has studied Computer Engineering at the Technical University Dresden. In 1993 he received his diploma degree and joined the Fraunhofer Institute for Integrated Circuits in Dresden. His research interests are modeling and simulation of complex mixed-signal systems and methodologies for a seamless design-flow.

J.P.M. Voeten received his master's degree in Mathematics and Computing Science in 1991 and his Ph.D. in Electrical Engineering in 1997 from the Eindhoven University of Technology. Since 1997 he is assistant professor in the section of Information and Communication Systems. His research interests include formal techniques for the design, specification, analysis and implementation of communicating hardware/software systems.



P.H.A. van der Putten received his degree in Electrical Engineering from the IHBO in Eindhoven. Since 1974 he was research employee at the section Digital Systems. In 1993 he received his degree Master of Technological Design from the Stan Ackermans Institute (TU/e). Since 1993 he is assistant professor in the section of Information and Communication Systems. In 1997 he received his Ph.D. from the Eindhoven University of Technology. His research interests include requirements analysis, object-oriented analysis, design methodology, and system level modeling of hardware/software systems.



Nigel Bleasdale was born in Chester, United Kingdom in 1960. He received the BSc degree in Electrical and Electronic Engineering from Salford University, England in 1983. From 1983 to 1998 he worked at Ferranti Electronics which later became Plessey Semiconductors as a semi-custom analog design engineer. The last four years were spent in leading a design group for Mass Storage integrated circuits. He is currently with Antrim Design Systems Inc., Scotts Valley, California with responsibilities for verilog-A model development and consulting services.

Frank Ghenassia
Education:
1893: Diplome d'ingenieur, Lyon France
1995: Master of Science, Haifa, Israel
Experience:
1994 - 1995: IBM Israel, development of software compilation tool
1995 - 1996: ST UK, development/porting of operating systems
1996 - 2002: ST France, development of software debugger tool and system2RTL design and verification flow



Alain Vachoux is a Principal Research Engineer in the Microelectronic Systems Laboratory of EPFL, the Swiss Federal Institute of Technology in Lausanne, Switzerland, where he is working on design flows and methodologies and the use of languages for analog and mixed-signal design. He previously held positions in industry in Xemics, a fabless semiconductor company, and in Antrim Design systems, an EDA company.



Masahiro Fujita received his Ph.D. degree in Engineering from the University of Tokyo in 1985 and shortly after joined Fujitsu Laboratories Ltd. From 1993 to 2000, he had been assigned to Fujitsu's US research office and directed the CAD research group. In March 2000, he joined the department of Electronic Engineering in the University of Tokyo as a professor. He has written over 100 technical papers on all aspects of logic design CAD. He has received several awards from Japanese major scientific societies on his works in formal verification and logic synthesis. His doctor degree thesis was written in early 80's and on model checking. Since then he has been involved in many research projects on various aspects of formal verification.



Rainer Doemer obtained his Diploma in Information and Computer Science from the University of Dortmund, Germany, in 1995. He continued his studies as a researcher in Computer Science at the University of Irvine, California, and received the Ph.D. degree from the University of Dortmund, Germany, in 2000. Presently he is working as a Research Specialist at the Center of Embedded Computer Systems at UCI. He is the lead developer of the SpecC Reference Compiler and Simulator.



Ralph-Johan Back is a Professor of Computer Science at Åbo Akademi University, Finland and Director of the Turku Centre for Computer Science. His research interests include program specification, refinement and verification, programming languages, programming environments, distributed, parallel and hybrid systems, object oriented programming, UML-modelling and software engineering. He is the inventor of the refinement calculus, a comprehensive mathematical framework for the development of programs, including concurrent and interactive programs.



Michael Goldsmith is Managing Director of Formal Systems (Europe) Ltd (www.fsel.com), the company which developed the FDR model-checker for CSP. His research concerns the application of mechanical analysis to aspects of distributed systems and communication networks, particularly security protocols for key-exchange and authentication. He is also a Senior Research Fellow of Worcester College, Oxford.

... Planning

TIME	Tuesday 24	Wednesday 25	Thursday 26
8h30			
9h00	AMS tutorial	AMS S2	AMS tutorial
	UML tutorial	UML S2	AMS tutorial
	SOPHOCLES workshop	Accellera	AMS tutorial
10h30			
	BREAK	BREAK	
11h00	AMS tutorial	AMS S3	AMS tutorial
	UML tutorial	UML S3	AMS modeling
	SOPHOCLES workshop	Accellera	AMS modeling
13h00			
	LUNCH	LUNCH	
13h30			
14h00	AMS tutorial	AMS S4	BEAMS Open Meeting
	UML tutorial	UML S4	BEAMS Open Meeting
	SOPHOCLES workshop	Accellera	BEAMS Open Meeting
15h30			
	BREAK	BREAK+POSTERS	BREAK
16h00	AMS S1	AMS S5	
	UML S1	UML S5	
	SOPHOCLES workshop	Accellera	
17h30			
18h00			
20h00		SOCIAL EVENT	



Meetings on-site

Thursday 26		Friday 27		TIME
CSD Opening & invited session	SFP tutorial	CSD tutorial Invited Talks I	SFP S2	8h30
				10h15
BREAK		BREAK+POSTERS		
CSD S1	SFP tutorial	CSD tutorial Invited Talks II	SFP S3	10h45
				12h30
LUNCH		LUNCH		
CSD S2	SFP Opening & invited session	CSD S4	SFP S4	13h30
				15h15
BREAK		BREAK		
BREAK+POSTERS		CSD S5	SFP S5	15h30
CSD S3	SFP S1			16h30
		CLOSING SESSION		17h00

Tuesday 24th, September

System Level Design DWG - VSI Alliance

B. Bailey

ODETTE Project Meeting (E.U.) (Members only)

Partners: OFFIS, IBM Israël, LEDA, Siemens ICN, ECSI

Wednesday 25th, September

PUSSEE Project Meeting (E.U.) (Members only)

Partners: Volvo, Nokia, Intracom, Univ. of Southampton, Clearsy, KeesDA, Univ. of Paderborn

Friday 27th, September

VC Quality DWG - VSI Alliance

P. Bricaud



**Set-up your
European
meeting
in conjunction
with FDL'02**

*(free facilities
for registered
attendees)*

... Tuesday 24th, September

AMS

9H00- TUTORIAL 10H30

Modeling and Simulation of Mixed-Signal Systems with SystemC (1st part)

Karsten Einwich, FhG IIS-EAS Dresden, Germany

Christoph Grimm, Univ. Frankfurt/Technische Informatik, Germany

State of the art mixed-signal system on chip solutions become more complex in respect of the interaction of different system parts such as analog environment and front-end, filters, converters, dsp algorithm, control algorithm and logic. To manage this tight linkage, an overall system simulation on different abstraction levels is essential.

For digital domains, SystemC seems to become the standard for system specification, simulation and refinement. However, the SystemC methodology currently considers digital domains only. This tutorial shows possibilities for modeling of mixed-signal behaviour using the currently available SystemC version. Within the tutorial, the use and coupling of different digital and analog „Models of Computation“ is shown. Furthermore, the concepts for extension of SystemC for simulation of analog and mixed-signal systems developed by the Mixed Signal SystemC study group are presented and demonstrated on the basis of first prototype implementations for the necessary reference library. Finally, concepts for an integration of a SystemC based mixed signal methodology in a seamless design-flow are presented.

10H30- COFFEE BREAK 11H00

11H00- TUTORIAL 13H00

Modeling and Simulation of Mixed-Signal Systems with SystemC (2nd part)

Karsten Einwich, FhG IIS-EAS Dresden, Germany

Christoph Grimm, Univ. Frankfurt/Technische Informatik, Germany

UML

9H00- TUTORIAL 10H30

System Level Modeling: from UML to executable models (1st part)

Dr. Ing. P.H.A. van der Putten, Dr.ir.J.P.M. Voeten

The tutorial gives an introduction to emerging new approaches for system level design of complex hardware/software systems. The trend that products and systems become communicating systems, with many parallel activities on multiple embedded processors, and with complex multimedia interfaces makes their design unmanageable with the current hardware/software co-design practice. This workshop presents a system level design approach that yields executable system level models starting from a UML specification. The models formalize functional real-time behavior as well as system architecture. This enables verification and validation of required system properties. Dedicated models can be used for architecture studies on performance, channel bandwidths and real-time properties. Descriptive models can be used for automatic synthesis of real time systems.

10H30- COFFEE BREAK 11H00

11H00- TUTORIAL 13H00

System Level Modeling: from UML to executable models (2nd part)

Dr. Ing. P.H.A. van der Putten, Dr.ir.J.P.M. Voeten

SOPHOCLES

9H00- THE ENVIRONMENT 10H30

Chair: AM. Fouilliant, THALES Communications France

ITEA project SOPHOCLES, System level development Platform based on Heterogeneous models and Concurrent Languages for System applications implementation, will provide designers with a high-level modelling platform for real time complex system design.

This session will give an overview of the Sophocles project.

SOPHOCLES Environment

D. Ragot, THALES Communications

Sophocles Virtual Enterprise

- Cyber Enterprise Model

F. Fontana, ENEA

- Global design IPK framework and Intelligent Cognitive Advisor

A.M. Gadamski, ENEA

10H30- COFFEE BREAK 11H00

11H00- TECHNICAL ISSUES (1) 13H00

Chair: P. Kajfasz, THALES Communications France

Introduction

D. Ragot, THALES Communications

Multiformalism and Proof on Control (invited presentation)

F. Boulanger, Ecole Supérieure d'Electricité

Untimed distributed Simulations

- ARRAY-OL formalism

A. Demeure, THALES Underwater Systems

- Gaspard environment

JL. Dekeyser, Laboratoire d'Informatique Fondamentale de Lille

- Yapi and its distributed simulation within the Sophocles environment

F. Theeuwens, Philips

UML ARRAY-OL for Signal Processing

C. Dumoulin, Laboratoire d'Informatique Fondamentale de Lille

13H00-14H00 LUNCH



AMS

14H00 OPENING SESSION

14H30- INVITED PAPERS 15H30

Chair: P. Schwarz, Fraunhofer IIS, Germany

Co-Chair: A. Vachoux, EPFL, Switzerland

Continuous, discrete and mixed-signal simulation is a big challenge for design automation. In the papers, these problems are discussed in the context of design flow, modeling methodology, and numerical simulation algorithms. Special requirements result from a broad range of application areas, from microelectronics, telecommunications to mechatronics and automation systems.

Mixed-signal Design Issues

G. Gielen, KUL, Belgium (TBC)

Tentative second paper

E. Christen, Avant!, US (TBC)

15H30- COFFEE BREAK 16H00

16H00- SESSION 1: 17H30 IP REUSE

Chair: R. Seepold, FZI, Germany

Co-Chair: R. Wittmann, Nokia, Germany

IP Reuse is often focussed to the digital domain. However, the amount of systems that contain analog and mixed-signal components is increasing. This session gives an overview of actual approaches to the reuse of analog and mixed-signal components.

IPCHL - A Description Language for Semantic IP Characterization

M. Schaaf, M. Visarius, R. Bergmann, R. Maximini, M. Spinelli, J. Lessmann, W. Hardt, S. Ihmor & W. Thronicke

Behavioural Library Development : Models Documentation and Qualification

N. Milet-Lewis, S. Snaidero, Y. Hervé, G. Monnerie, D. Geoffroy, A. Fakhfakh & H. Levi

Multi-level analog/mixed-signal IP specification

N. Martinez-Madrid

UML

14H00- OPENING SESSION 15H30 & INVITED PAPERS

Chair: G. de Jong, Telelogi, Belgium

The speakers in this session will present the need for new design methodologies and flows for embedded systems. Particular attention will be given as how software systems and their development processes and methods bear many commonalities with the design of hardware and embedded systems, specifically in the context of architecture and platform based design paradigms.

Experiences from applying OO to DSP Development at Nokia

I. Olivier, Nokia

15H30- COFFEE BREAK 16H00

16H00- SESSION 1: 17H30 EMBEDDED SYSTEM DESIGN METHODOLOGIES

Chair: P. van der Putten, Eindhoven University of Technology, The Netherlands

This session will discuss the use of object-oriented design methodologies and will position the various OO concepts, diagrams and methods in a complete setting for the modeling, specification and design of embedded systems.

Embedded System Design Using UML and Platforms

R. Chen, M. Sgroi, L. Lavagno, G. Martin, A. Sangiovanni-Vincentelli & J. Rabaey

ModelJ: System-level model for embedded system design

R. Hamouche, B. Djafri & J. Benzakki

Invited paper: Critical Systems Development with UML

J. Jürjens

SOPHOCLES

14H00- TECHNICAL ISSUES (2) 15H30

Chair: F. Theeuwens, Philips Research The Netherlands

System Validation with Esterel Studio

L. Delamare, Esterel Technologies

Evolving Grammars formalism

S. Piria, IPITEC

SIMPLE a VC generation environment

P. Palazzari, ENEA

Magisim a Cycle accurate Simulator

A. Ricciardi, IPITEC

15H30- COFFEE BREAK 16H00

16H00- DEMONSTRATIONS 17H30 SESSION

Chair: P. Palazzari, ENEA Italy



.. Wednesday 25th, September

AMS

8H30- SESSION 2: 10H30 MODELING TECHNIQUES

Chair: A. Vachoux, EPFL, Switzerland
Co-Chair: A. Rueda, Inst. of Microelec. Sevilla, Spain
Analog and mixed-signal hardware description languages offer a large spectrum of capabilities when it comes to describe the behavior of electronic systems. The first presentation aims at comparing two implementations of an opto-electronic interconnection circuit with the VHDL-AMS and the Verilog-AMS languages. The second presentation describes a process to generate nonlinear models of mixed-signal circuits based on circuit characterization and model tables. The third presentation deals with modeling guidelines for efficient synthesis of synchronous counters.

VHDL-AMS and Verilog-AMS as Competitive Solutions for the High Level Description of Thermodynamical Interactions in Opto-Electronic Interconnection Schemes

F. Pecheux & C. Lallement

A new approach to model generation for nonlinear mixed-signal circuits in the behavioural and functional domain

R. Rosenberger & S. A. Huss

Synthesizable High-Speed Synchronous Counters of Arbitrary Width

H. Gustat & F. Winkler

The BEAMS Association

N. Millet-Lewis or Y. Hervé

10H30- COFFEE BREAK & 11H00 POSTERS

11H00- SESSION 3: 13H00 MODELS OF COMPUTATION

Chair: C. Grimm, Univ. of Frankfurt, Germany
Co-Chair: N. Martinez-Madrid, FZI, Germany

Abstract modeling and Simulation of mixed-signal systems is still a challenge. This session presents approaches to describe such systems in an abstract way within different models of computation. The presentations give an overview of ongoing activities for mixed-signal extensions to SystemC and on Modelica. Further presentations describe an approach to mixed-signal time/frequency simulation with VHDL-AMS and the generation of efficient code from Simulink.

Mixed-Signal Extensions for SystemC

K. Einwich, P. Schwarz, Ch. Grimm & K. Waldschmidt

Mdl2dag: Convert Graphical Model System Files to DAGs

M. Solar & M. Feeley

An Approach to Mixed Time/Frequency Simulation and VHDL-AMS Extensions

N. Parthasarathy, S. Raghuram, W.F. Chen & H.W. Carter

Mixed Domain Modeling & Simulation in Modelica

C. Clauss, H. Elmquist, S.E. Mattsson, M. Otter & P. Schwarz

UML

8H30- SESSION 2 : 10H30 UML REAL-TIME PROFILES

Chair: J. Van Sas, Alcatel, Belgium

This session will present an in-depth overview of the upcoming UML 2.0 specification, which will provide the infrastructure, formal modeling and analysis capabilities required to support the analysis and design of real-time systems. The second contribution will give a concrete example of those real-time profile features present in UML 2.0.

Support for embedded systems in UML 2.0.

M. Björkander & C. Kobryn

An UML profile for real-time system modeling with rate monotonic analysis

I. Oliver

10H30- COFFEE BREAK & 11H00 POSTERS

11H00- SESSION 3 : 13H00 SYNTHESIS AND IMPLEMENTATION FROM UML

Chair: G. de Jong, Telelogic, Belgium

This session will first present examples of UML's extension mechanisms used towards the synthesis and implementation of hardware and embedded systems. The presentations will be followed by a general discussion on the differences and commonalities between the presented real-time profiles and stereotypes, with the aim to conclude on a commonly agreed set of required concepts.

SystemC code generation from UML models

F. Bruschi, E. di Nitto & D. Sciuto

Platform modeling with UML and SystemC

P. Green & M. Edwards

On practical usage of stereotypes in UML-software development

L. Kuzniarz & M. Staron

HDL Procedural Interface Modeling using UML

F. Martinolle & J. Bhasker

ACCELERA

8H30- ROSETTA & 10H30 SYSTEMVERILOG TUTORIAL

Chair: V. Gerousis, Infineon, Germany

In this tutorial, an introduction to Rosetta and SystemVerilog will be given. Rosetta as the system-level language and SystemVerilog as the architectural design and verification language. The tutorial will point out the semantic foundation of both languages.

Rosetta: The System-Level Language

P. Alexander, University of Kansas, USA (TBC)

SystemVerilog: The Architectural Design Language

P. Flake, Co-Design, UK

10H30- COFFEE BREAK 11H00

11H00- REUSABILITY 13H00

Chair: P. Alexander, University of Kansas, USA (TBC)

In this session the VSIA initiatives towards facilitating system-level integration of virtual components will be addressed. Both interface modelling and System verification reuse will be discussed.

Interface Technology

B. Bailey, Mentor Graphics, USA

Verification Reuse Enables Design Reuse

T. Anderson, O-In Design Automation, USA

13H00-14H00 LUNCH



AMS

14H00- SESSION 4: 15H30 APPLICATION EXAMPLE

Chair: R. Wittmann, Nokia, Germany
Co-Chair: Y. Hervé, Univ. Strasbourg, France

The VHDL-AMS language becomes more and more used in practical applications as a unified medium for the design of complex systems. The first three presentations in this session give detailed examples of such a fact in the domains of power electronics, digital TV, and mobile telephony. The last presentation provides a first user perspective on how to put the VHDL-AMS language at works.

Modeling and simulation of power electronics systems using VHDL-AMS: A methodology proposal
D. Glao & S. Garcia-Sabiro

ADMS in digital TV applications
B. Le Chapelain

Full Transceiver Circuit Simulation using VHDL-AMS
J. Oudinot, S. Scotti, J. Ravatin, A. Le-clercq & J. Lebrun

Modeling in VHDL-AMS - New Users First Experience
B. Anderson & R. Munden

15H30- COFFEE BREAK 16H00 & POSTERS

16H00- SESSION 5: 17H30 MIXED DOMAIN APPLICATION

Chair: E. Moser, Robert Bosch, Germany
Co-Chair: P. Schwarz, FHG IIS, Germany

Modern modeling languages offer the possibility to describe multi-physics or multi-domain problems. These possibilities are investigated in the context of micro-electro-mechanical systems (MEMs), mechatronics (including hydraulics & magnetics), and electro-optical devices. These applications are typical examples of actual design problems.

VHDL-AMS in MEMS Design Flow
J. Haase, J. Bastian & S. Reitz

Study of a Mechatronic Valve Model for the Automotive Industry
C. Meise, P. Oehler, S. Beitschuh, W. Feyl & G. Schmitz

A VHDL-AMS Spectral Model of Photodetectors for Active Pixel Sensors
F. Dadouche, A. Alexandre, B. Granado, A. Pinna & P. Garda

UML

14H00- SESSION 4 : 15H30 UML AND SEMANTICS

Chair: J. Voeten, Eindhoven Univ. of Technology, The Netherlands

The presentations in this session will provide illustrations of UML compliant action languages, and other examples of formal semantic embeddings in UML. Furthermore, a forum will be given to discuss formal semantics of UML.

Developing Embedded Systems Using Model-Driven Architectures and Executable UML
C. Raistrick

Using the SHE Method for UML-based Performance Modeling
B.D. Theelen, P.H. A Van der Putten & J.P.M. Voeten

Real-time multitask design based on SDL
A. Alkhodre, J.P. Babau & J.J. Schwarz

15H30- COFFEE BREAK 16H00 & POSTERS

16H00- SESSION 5: 17H30 UML-BASED DESIGN FLOWS AND EXPERIENCES

Chair: M. Edwards, Univ. of Manchester, UK

This session will present a set of new and UML based design flows defined in industrial contexts. The presenters will share their experiences in applying these new flows to real-life industrial applications and novel architectures.

A design methodology for the development of a complex SoC using UML and executable system models
Y. Vanderperren, G. Sonck, P. Van Oostende, M. Pauwels, W. Dehaene & T. Moore

HW dependent SW, the bridge between HW & SW : A Generic Handler Framework
R. Marichal & J. Van Sas

UML-driven TTA-based protocol processor design
J. Lilius & D. Truscan

ACCELERA

14H00- PANEL SESSION: 15H30 WHO CARES ABOUT SYSTEM VERIFICATION?

Moderator: V. Gerousis, Infineon, Germany

In this panel, system-level verification will be analysed. Open questions such as:

- Can C/C++ improve system-level verification?

- Is it really needed a separate verification language?
- Why can't verification engineers get respect?

will be made to the panellist and the audience and their positions discussed.

Panelists

P. Alexander, University of Kansas, USA (TBC) - P. Flake, Co-Design, UK - B. Bailey, Mentor Graphics, USA - C. Eisner, IBM, USA - W. Rosenstiel, FZI, Germany - M. Fujita, University of Tokyo, Japan

15H30- COFFEE BREAK 16H00

16H00- ECSI/ACCELERA 17H30 SESSION

Chair : I. Phillips, ARM, UK
Scriber: K. Tiensyrja, VTT, Finland

Working Session: System-level languages and taxonomy

This working session will analyse the different system-level languages currently proposed. Patrizia Cavalloro, from Italtel, will present the Sydic-Telecom taxonomy as a starting working document. After her presentation, the taxonomy will be discussed and the following open questions will be translated to the audience:

- What are the main characteristics required for a system-level language?
- Can we list languages that are claimed to be system-level?
- Where fit these languages in the puzzle in terms of verification, synthesis, constraints and architecture specification ?

The most relevant results of the discussion will be written down by the scribe who will make a summary of the session results at the end.

.. Thursday 26th, September

AMS

8H30- TUTORIAL 10H30

Mixed-Signal Modeling with VHDL-AMS and Verilog-AMS (1st part)

Alain Vachoux, EPFL, Microelectronic Systems Lab., CH

Nigel Bleasdale, Antrim Design Systems, US

This tutorial aims at providing practical modeling techniques for mixed-signal design with examples in both the VHDL-AMS and the Verilog-AMS languages. The tutorial covers continuous time, event-driven, mixed-signal, testbench and silicon-calibrated behavioral modeling techniques. Several meaningful and highlighting practical examples are given. The tutorial is not an introduction to the VHDL-AMS and Verilog-AMS languages per se, although it does present key aspects of these languages as an introduction. The tutorial aims at showing that there are common underlying semantics that can be expressed in two different, but equivalent ways.

10H30- COFFEE BREAK 11H00

11H00- TUTORIAL 13H00

Mixed-Signal Modeling with VHDL-AMS and Verilog-AMS (2nd part)

Alain Vachoux, EPFL, Microelectronic Systems Lab., CH

Nigel Bleasdale, Antrim Design Systems, US

CSD

9H15- OPENING & 10H30 INVITED SESSION

Chair: E. Villar, Univ. of Cantabria, Spain

CSD introduction

W. Rosenstiel, Univ. of Tuebingen, Germany

System-level Design Based on C/C++ : "What is needed and what is not"

D. Gajski

10H30 COFFEE BREAK

11H00- SESSION 1: 13H00 MULTILANGUAGE APPROACH TO DESIGN FLOW

Chair: W. Rosenstiel, Univ. of Tuebingen, Germany

System design needs languages to allow descriptions of all design phases. This session will discuss the possibility of using multi-language approaches, showing how existing methodologies and tools are used and combined in order to cover the complete design flow, with particular emphasis for high level design.

C/C++ Based System Design Flow Using SpecC, VCC and SystemC

M. Olivarez

High-level design of soft IPs using C++ and SystemC

M. Damazevicous & V. Stuikeys

Java Data Flow for Real-Time HW/SW of Mobile Devices

R. Hualmé, J.-P. Babau & A. Mignotte

Verification of Synchronization in SpecC Description with the Use of Difference Decision Diagram

T. Sakunkonchak & M. Fujita

SFP

8H30- TUTORIAL 10H30

Introduction to CSP and FDR (1st part)

M. Goldsmith, Formal Systems (Europe) Ltd

The theory of refinement with foundations in the model of concurrency based around Hoare's CSP (Communicating Sequential Processes), allows a wide range of correctness conditions, including deadlock and livelock freedom as well as general safety and liveness properties, to be encoded (using standard idioms) as a comparison between processes. FDR (Failures-Divergence Refinement) allows the checking of many properties of finite-state systems and the investigation of systems which fail these checks. It is based on the theory of Communicating Sequential Processes developed at Oxford University and applied successfully in a number of industrial applications. Its method of establishing whether a property holds is to test for the refinement of a transition system capturing the property by the candidate machine. There is also the ability to check determinism of a state machine, and this is used primarily for checking security properties.

10H30- COFFEE BREAK 11H00

11H00- TUTORIAL 13H00

Introduction to CSP and FDR (2nd part)

M. Goldsmith, Formal Systems (Europe) Ltd

13H00-14H00 LUNCH

CSD

14H00- BEAMS OPEN 15H30 MEETING

BEAMS is a non-lucrative association of researchers, engineers, companies, teachers or students whose objective is to promote behavioural modelling and simulation, for the design of analogue, mixed and multi-technological systems, mainly using the standard language VHDL-AMS.

Because the future SOC imposes a questioning of the traditional design methods, especially in the analogue and mixed domain, because Top-Down design, design Re-use, IP-based design are emerging solutions and because all may have a common denominator which is VHDL-AMS, BEAMS proposes to link various experiments to share new ideas, methodologies, techniques, libraries of IP models, training programs, etc.

Let visit our web site :
<http://www.beams.asso.fr>



14H00- SESSION 2: 15H30 DIFFERENT ASPECTS OF PLATFORM BASED DESIGN

Chair: *M. Fujita*, Univ. of Tokyo, Japan

Different approaches for platform based evaluation and HW/SW co-design in SystemC, modeling of memory subsystems, as well as testbench aspects will be presented.

System-based Performance Estimation of Multi-processing, Multi-threading SoC Networking Architectures

N. Pazos, W. Brunnbauer, J. Foag & T. Wild

HW/SW interface implementation of SystemC for platform-based design

F. Herrera, P. Sánchez & E. Villar

Using Esterel & C for High-Level Modelling of Memory Subsystems in SOCs (S)

M. Gumm, C. Schmid, G. Placido, Andre Chatelain, Y. Mathys & A. LaRosa

IMEM: An OO memory and interface modeling approach for RT video-processing systems (S)

B. Thörnberg, H. Norell & M. O'Nils

Testbench Support for SystemC Specifications (S)

A. Braun, C. Hansen, J. Gerlach & W. Rosenstiel

15H30- COFFEE BREAK 16H00 & POSTERS

16H00- SESSION 3: 17H30 RTOS MODELING AND SOFTWARE GENERATION

Chair: *M. Radetzki*, SCI Works, Germany

This session deals with HW/SW co-design of embedded systems. The first paper describes mapping of SW onto an RTOS from aspect oriented specification. Based on an extended task graph, the second paper explains how a scheduled and executable SystemC model is generated. The third paper presents a methodology for modeling a priority-based preemptive RTOS kernel in SystemC.

An aspect-oriented approach making auto-generated code for embedded RT-Systems retargetable

T. Maier-Komor

Automatic generation of scheduled SystemC models of embedded systems from extended task graphs

S. Klaus, S. A. Huss & T. Trautmann

A SystemC Model for RTOS Kernel

M. Abd-El-Salam & A. Salem

SFP

14H00- OPENING 15H30 & INVITED SESSION

Chair: *T. Lecomte*, ClearSy, France

SFP Introduction

M. Butler, Univ. of Southampton, SFP chair.

Keynote speech : reasoning about Interactive Systems

R.-J.R Back, Åbo Akademi, Finland.

This talk will show how contracts may be used to model and reason about interactive systems. A contract is a way of describing the behaviour exhibited by a collection of possibly competing agents. It is possible to analyse whether an agent or coalition of agents can achieve a certain goal even in the presence of hostile behaviour from other agents. It is shown how to analyse whether a coalition of agents can enforce a certain temporal behaviour when executing a contract. Illustrative examples will be used to show how to model and analyse interactive systems using this approach.

15H30- COFFEE BREAK 16H00 & POSTERS

16H00- SESSION 1: 18H00 HARDWARE-ORIENTED SYSTEM DESIGN

Chair: *L. Pierre*, Univ. of Provence, France

This session is concerned with formal approaches to hardware design. Approaches supporting refinement, transformation and property checking of hardware designs are presented.

Formalizing configuration relocation behaviors for reconfigurable computing

P.C. Vinh & J.P. Bowen

Asynchronous Circuit Design via Automated Petri Net Generation

D. Furey & M. B. Josephs

Specification and Refinement of Hardware Components in B

S. Hallerstede

"Sugar" a Formal Property Language

A. Ziv, IBM

CSD

SFP

8H30-10H15 TUTORIAL/INVITED TALKS I

Chair: *W. Rosenstiel*, Univ. of Tuebingen, Germany

Early embedded software development using SystemC-based TLM models

F. Ghenassia, ST Microelectronics, France

Embedded software accounts for more than half of the total development time of a system-on-a-chip. The critical path for the development of such circuit is consequently often the software, not the hardware. Enabling software development to start very early in the development cycle is therefore of paramount importance to reduce the time-to-market. In this talk, I will describe our SystemC-based methodology to support this new challenge and focus on the usage of a Transaction-Level Model (TLM) abstraction layer that describes SoC architecture at a level suitable for early software development and architecture analysis. The design of a multimedia platform will be presented as an illustration of the benefits of such approach.

10H15-10H45 COFFEE BREAK & POSTERS

10H45-12H30 TUTORIAL/INVITED TALKS II

Chair: *N. Fristacky*, Slovak Univ. of Technology, Slovakia

SpecC language version 2.0: C-based system design language that covers from RTL to embedded software

M. Fujita, Univ. of Tokyo, Japan

R. Doemer, Univ. of California, Irvine, US

SpecC is a C-based system level design language originally developed by Prof. Gajski's research group. It is now open and standardized from SpecC Technology Open Consortium (STOC <http://www.specc.gr.jp/eng/index.htm>). SpecC-based design methods provide seamless connection of specification and design steps for SOC (System on Chip) designs through collaboration among embedded software tool vendors, electronics design automation tool vendors, and systems integrators. SpecC version 1.0 was established in March 2001. Now its major version upgrade, version 2.0 will be available this spring. In version 2.0 there are several important issues that have been accommodated:

- (1) A new set of language constructs that gives very efficient and easy-to-understand RTL description styles is introduced. Now SpecC covers from embedded software to RTL (real hardware)
- (2) Semantics of the constructs for parallelism and synchronization are rigorously defined. Now SpecC is well-defined even in mathematical sense.
- (3) Many syntactic and some semantics issues raised from the real use of SpecC have been resolved.

Reference compiler for SpecC version 2.0 will be released early summer. In this tutorial, after introducing basic ideas of SpecC language and its design methodology, we will describe details of the key issues of SpecC version 2.0

8H30-10H15 SESSION 2: EMBEDDED SYSTEM DESIGN

Chair: *R. Passerone*, Cadence, US

This session is concerned with design approaches for embedded systems. Modelling approaches for system level design with a formal basis are presented. Support for the design process is also addressed.

Invited Paper: Integration of the proof process in the system development through refinement steps

D. Cansell & D. Mery

A New Modeling Approach Towards System-Level Design-Space Exploration

F.N. van Wijk, J.P.M. Voeten & A.J.W.M. ten Berg

Ensuring semantic integrity in knowledge bases for embedded systems

D. Monjau & M. Sporer

Poster presentations

10H15-10H45 COFFEE BREAK & POSTERS

10H45-12H30 SESSION 3: PARALLELISM & MODELS OF COMPUTATION

Chair: *J. Mermet*, Keesda, France

This session is concerned with parallelism and models of computation. The design and exploitation of parallelism for improved performance is addressed using formal frameworks. An approach for representing models of computation is also presented.

Invited paper: Modeling Techniques in Design-by-Refinement Methodologies

J.R. Burch, R. Passerone & A.L. Sangiovanni-Vincentelli

Design of highly parallel architectures with Alpha and Handel

F. D. de Dinechin, T. Risset, M. Manjunathaiah & M. Spivey

MTG* and Grey-Box: modeling dynamic multimedia applications with concurrency and non-determinism

S. Himpe, G. Deconinck, F. Catthoor & J. van Meerbergen

MCML-A markup language for a model-of-computation centred design and verification environment

J. Levihn, M. Krieger, H. Eveking & C. Blank

13H00-14H00 LUNCH



13H30-15H00 SESSION 4: OBJECT-ORIENTED EXTENSIONS TO SYSTEMC FOR MODELING & SYNTHESIS (ODETTE)

Chair: *M. Bombana*, Siemens ICN, Italy

Modeling & verification of complex systems require the adoption of object-oriented features, like class hierarchy, polymorphism and improved communication, without losing the chance of adopting synthesis to reach implementation. In this session, proposed extensions to SystemC are presented, with modeling experiences from two different application domains.

Invited paper: SystemC object-oriented extensions & synthesis features
E. Grimpe

SystemC-plus complex data types for telecom applications
M. Bombana, W. Fornaciari & L. Pomante

Object-Oriented High-Level Modeling of an InfiniBand to PCI-X Bridge
O. Lachish & A. Ziv

15H00-15H15 COFFEE BREAK
15H15-16H30 SESSION 5: EXTENSION OF C-BASED DESIGN LANGUAGES

Chair: *A. Morawiec*, ECSI, France

This session is devoted to present the extensions proposed to the existing C-based design languages. It is expected that these extensions will, on one hand, enable to cover higher levels of abstraction by combining some language constructs from various languages like Esterel and C. On the other hand, some improvements are proposed to the existing standards (e.g. SystemC), that allow for a coherent design flow from specification to implementation.

A study of specification experiments with ECL
L. Ribas & J. Saiz

A method for the development of combined floating- and fixed-point SystemC models
Y. Vanderperren, W. Dehaene & M. Pauwels

Handel-C for co-processing and co-design of System on programmable ship (SoPC)
C. Sullivan, Celoxica

13H30-15H00 SESSION 4: MATISSE PRESENTATIONS

Chairs: *K. Kronlöf*, Nokia, Finland

This session give an overview of the EU-funded IST project MATISSE (Methodologies and Technologies for Industrial Strength Systems Engineering). MATISSE makes extensive use of the B Method and includes several significant industrial partners who are exploiting B.

The Use of B for Smart Cards
J.-L. Lanet, Gemplus

Combining UML with B
C. Snook, University of Southampton

System Modelling with Event B
T. Lecomte, ClearSy

15H00-15H15 COFFEE BREAK
15H15-16H30 SESSION 5: PANEL ON REFINEMENT

Chairs: *M. Butler*, University of Southampton, UK

Participants will include:
M. Butler, R.-J. Back, M. Goldsmith, J.L. Lanet, T. Lecomte


16H30-17H00 LOTTERY AND CLOSING SESSION

... General Information

LOCATION

The Forum will be held in Marseille.
Founded by the ancient Phocian Greeks, Marseille has been a thriving port city for over 2000 years. It is France's oldest city and one of its most colourful. The influence of labourers from Italy, Greece, Corsica and North Africa dominates much of the city's sensual spirit, which is centred around the picturesque Vieux Port and its outdoor markets.
The Forum will be held at the ESIM, which is located in the north/west of Marseille, in the Technopôle de Château Gombert, rue Joliot Curie.

LANGUAGE

The language of the Forum will be English.

REGISTRATION

The Registration Desk is located in the lobby of the "ESIM" Building. Registration hours are the following:

	Forum	Hands-on Labs
Mon. 23	14:00-18:00	17:00-18:00
Tues. 4	8:00-18:00	id
Wedn. 5	8:00-18:00	id
Thurs. 6	8:00-18:00	id
Fri. 7	8:00-8:30	id

TECHNICAL PROGRAMME

The full Forum programme will start on Tuesday September 24, 2002 at 8h30 with the first tutorials. Then, other tutorials and technical sessions will follow until Friday, September 27, 2002. A number of hands-on labs will be provided in parallel with technical sessions.

CO-LOCATED MEETINGS

Scientific and technical meetings co-located with the conference are welcome.
Available time slots are: Monday and evenings, except on Wednesday
Requests should be sent to the secretariat and will be satisfied only if the benefit to the conference is clear.

HOTEL ACCOMMODATION

Delegates are kindly requested to make their hotel reservations by contacting the hotels directly. See the Web site for some information on hotels.

SOCIAL EVENTS

A Forum Diner will take place on Wednesday September 25. Participation to the Forum Dinner is only included in the 5 and 3 days Forum registration fee. Extra tickets may be purchased separately (40 Euros) within the limit of the boat's size.

UPDATED INFORMATION ON: www.ecsi.org/fdl02

FDL REGISTRATION

Attn. Florence Pourchelle - ECSI
Quartier Méridol Ouest
84550 MORNAS, France

Ph/Fx : +33 490 37 15 98
E-mail : florence.pourchelle@ecsi.org
Web : www.ecsi.org/fdl02

FDL ORGANIZATION

Groupe ESIM - CCIMP
Technopôle de Château-Gombert
13451 MARSEILLE Cedex 20

Web : www.esim.fr



Registration Form

FDL'02

Please complete this form and mail it or fax it with the proof of payment to: FDL '02 Secretariat
Attn. Florence Pourchelle Ph/Fx : +33 490 37 15 98
ECSI - Quartier Mérindol Ouest E-mail : florence.pourchelle@ecsi.org
F - 84550 MORNAS, France http://www.ecsi.org/fdl02

Attendee Information

Name (First, Last) Company
Address
City Post code Country
Email Phone Fax
Member of Member Nr.
Date Signature

Forum Registration Fees

Forum Fees	Received by August 24, 2002			After August 24 or on-site			Amount
	Member ECSI	Sponsors(1)	Non member	Member ECSI	Sponsors(1)	Non member	
Member							
5 days	395	435	485	445	490	540	
3 days	340	370	400	370	405	440	
2 days (3)	260	280	300	290	310	340	
Students (2) & (3)	190			210			
Extra ticket for social event	40			40			
Total fee due							
V.A.T. 19,6 %							
Total Amount							

All Amount in Euros

Participation in the Monday meetings requires conference registration.
Notice of meetings on Monday will be added regularly to the web page: www.ecsi.org/fdl02

Method of payment

Bank transfer to: Crédit Agricole de l'Isère, 2 bvd des Alpes, 38240 MEYLAN Account #: 63275597000 - RIB Key: 06
Credit Card: VISA EUROCARD MASTERCARD
Credit card number: Expiration date:
Card holder (name as appearing on the card): Signature:

Registration instructions (one person per form)

(1) Members of sponsors include: Accelera, IFIP 10.5, ITG, GMM, GI, Mentor Graphics, Cadence, VDE, VSIA
(2) Students must provide a valid Student Identification.
(3) The students' fee and the 2 days' fee does not include the ticket for the social event: it has to be purchased separately
Note: no registration request will be confirmed until payment (or proof of payment) has been received
No registration will be accepted if received after August 24, 2002. After August 24, there will be on-site registration only.
Cancellation and Refund Policy: written requests for refunds must be postmarked no later than August 30, 2002. Refunds are subject to a 10% processing fee if received by August 30, a 50% fee if received after August 7. Requests for refunds received after the September 13, 2002 postmark date will not be honored and all registration fees will be forfeited.
V.A.T.: it will be charged only to citizens of the EEC and can be reimbursed to their company. However, in case of payment made directly by the company, V.A.T. is not charged, providing that they give their V.A.T. identification number.

V.A.T. Company ID number (if registration made by company):



... How to get to Marseille

Getting to Marseille by Train

Saint Charles Station

15 trains to Paris daily, including 12 TGV high-speed trains (3h00 journey)
<http://www.sncf.com>

Getting to Marseille by plane

Marseille Provence Airport (open 24 hours a day)
 Regular or charter flights between Marseille and 81 cities throughout the world
<http://www.marseille-provence.aeroport.fr>

Coach links between Marseille city centre and the airport :

Marseille to the airport
 From St. Charles Station
 Ph. : (+33) 4 91 50 59 34

Coaches : every 20 minutes from 6.10 a.m. to 9.50 p.m.
 Before 6.10 a.m. : 5.30 a.m. and 5.55 a.m.

From the airport to Marseille
 Ph. : (+33) 4 42 14 31 27

Coaches : every 20 minutes from 6.30 a.m. to 8.50 p.m.
 Before 6.30 a.m. : 6.15a.m.
 After 8.50 p.m. : 9.15 p.m. - 9.40 p.m. - 10 p.m. - 10.20 p.m. - 10.50 p.m.

In addition to the times mentioned above the bus service operates to serve incoming flights. The journey takes approximately 25 mins. Price : single tickets cost 7,16 euros (reduced prices for children and groups).

Taxis : 24 hrs. a day at the airport
 Ph. : (+33) 4 42 14 24 44

Taxis between the airport and Marseille city centre cost approximately 35/38 euros during the day and approximately 44/97 euros at night. The night rate is applicable between 7 p.m. and 7 a.m. and from midnight to midnight on Sundays and Public Holidays.

Co-sponsors



... How to get to ESIM

By Metro and Bus: metro M1 direction La Rose, and Bus line 1. Stop at IMT. By car: see map hereafter
More information and maps available on www.ecsi.org/fdl02

