

# DASC Presentation — FDL-2001

## **P1076 VHDL Analysis and Standards Group**

- *2000 Edition* approved: added protected types for shared variables
- 2001 revision in final recirculation before approval
- Collecting requirements for VHDL-200x

## **Issues Screening and Analysis Committee**

- Plans to address outstanding issues, forward LCSs to VASG for 200x.

## **VHDL Programming Language Interface Task Force**

- Aiming for internal draft end of 2001.

## **P1076.1 VHDL Analog and Mixed-Signal Working Group**

- Approved 1999.
- Working group considering minor enhancements to improve language usability
- Study group formed for standard packages for energy domains (elec, mech, thermal, etc)

## **P1076.2 VHDL Math Package Working Group**

- Approved 1996. Revision/reaffirmation review due to start.

## **P1076.3 VHDL Synthesis Package Working Group**

- Approved 1997. Revision review due soon. Proposal for synthesizable fix- and floating-point packages.

## **P1076.4 Timing (VITAL) Working Group**

- Revision approved 2000, now reviewing issues arising.

## **P1076.6 VHDL Synthesis Interoperability Working Group**

- Approved 1999: “lowest common denominator” subset
- Now working towards significantly expanded subset based on “in principle” synthesizability.

## **P1164 VHDL Multivalued Logic Packages Working Group**

- Approved 1993. Review in progress: minor enhancements, including I/O for std-logic types.

## **P1577 Object Oriented VHDL Working Group**

- Quiescent.

## **Lib IEEE Study Group**

- Seeking PAR to standardize what may go in library IEEE, to avoid incompatibility between vendors' tools.

### **VHDL Microwave Study Group**

- Developing proposal to extend VHDL & VHDL-AMS for high-frequency modeling.

### **P1029.1 Waveform and Vector Exchange Working Group**

- Revision approved in 1998. Working Group quiescent.

### **P1364 Verilog Working Group**

- Revision approved 2001: several language enhancements. In final editing phase.

### **P 1364.1 Verilog Synthesis Subset Working Group**

- Quiescent pending Verilog-2001 completion.

### **P1481 Circuit Delay and Power Calculation Working Group**

- Approved 1999. Working group meeting regularly to review and update work.

### **P1499 Open Modeling Forum Working Group**

- Approved 1998. Working group quiescent.

### **P1497 Standard Delay Format Working Group**

- Draft ready for submission to IEEE approval process.

### **P1551 VHDL System and Interface based Design Working Group**

- Quiescent

### **P1596 Advanced Library Format (ALF) Working Group**

- PAR approved 2001. Standardizing semantics of descriptions of technology-specific library cells. Functional, physical & electrical characteristics.

### **OpenAccess Study Group**

- Was CHDstd. Change of contributed technology (was IBM, now Cadence) lead to name change.
- Proposing standard API for accessing design data. Work in progress.